Multiple-Port Power Divider/Combiner Circuits Using Circular Microstrip Disk Configurations

MOHAMED D. ABOUZAHRA, SENIOR MEMBER, IEEE, AND KULDIP C. GUPTA, SENIOR MEMBER, IEEE

Abstract—**A generalized method for evaluating the scattering parameters of a multiport center-fed circular microstrip disk power divider/combiner circuits is presented. The method is based on the planar circuit approach in which the two-dimensional Green's function of a circular segment is used. Various symmetrical power divider/combiner circuits have been designed and tested. The effect of introducing additional shorted ports between the circumferential output ports on the reduction of spurious radiation losses is discussed. Experimental results verifying the design methodology are given.**

I. Introduction

SYMMETRIC N-WAY power dividers and power combiners have received considerable attention recently [1]–[4]. Due to their geometrical symmetry, these power dividers do not exhibit any imbalance in either the amplitude or the phase of the output signals at any frequency. This property makes them very attractive in many RF applications. Indeed, such power dividers have found extensive use in the design of multielement antenna feed systems. Also, multiple-port power combiners have been widely used in combining multiple oscillators or amplifiers in a single module [3], thus yielding higher output power capabilities.

Recently, the use of a circular microstrip center-fed disk structure as an N-way power divider/combiner has been reported [3], [4]. In the present paper, a generalized theoretical formulation and several experimental results for this new structure are presented. The geometry of this power divider/combiner circuit is illustrated in Fig. 1(a). At the center of the disk is a coaxially fed port which is the input port for a power divider or the output port for a power combiner. The other N ports are microstrip line ports symmetrically located around the circumference of the circular disk.

The theoretical analysis developed in this paper is based on the planar circuit approach which uses the two-dimensional impedance Green's function to derive the multiport impedance matrix. Since the center conductor diameter of the coaxial port is much smaller than the diameter of the disk, the Green's function of the circular disk geometry (rather than that of the annular ring geometry) has been used. This approximation has been found to be valid on the basis of the experimental verification discussed later. In order to optimize the design efficiently and to interpret the results, the impedance matrix is transformed into the more familiar scattering matrix representation. The validity

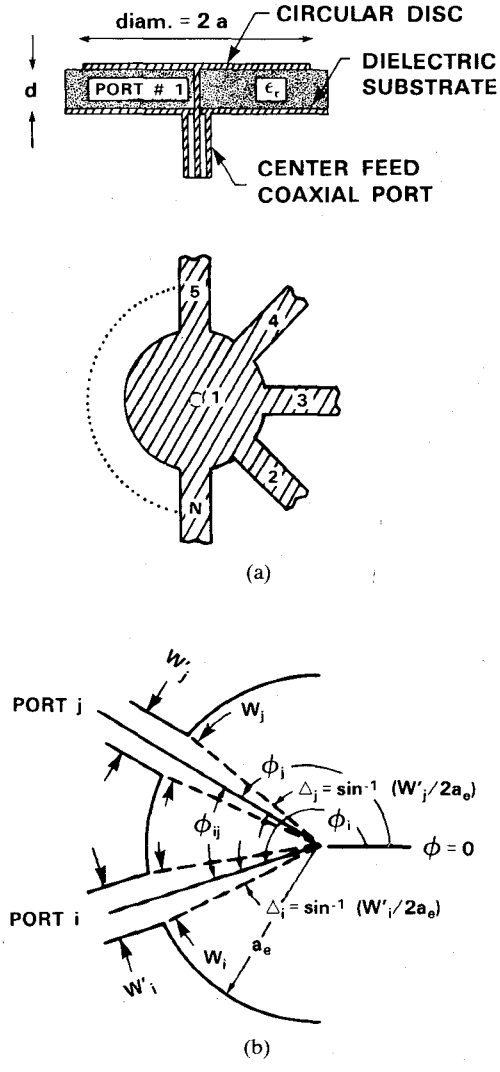

Fig. 1. (a) Circular microstrip disk structure with a single coaxially fed port at the center and $(N-1)$ microstrip ports along the circumference. (b) Parameters of the circumferential ports.

Manuscript received April 8, 1987; revised July 27, 1987. This work was supported in part by the Department of the Air Force.

M. D. Abouzahra is with MIT Lincoln Laboratory, Lexington, MA 02173.

K. C. Gupta is with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309.

IEEE Log Number 8717120.

of this approach and the feasibility of the design have been verified experimentally. The influence of introducing shorted ports (between the adjacent circumferential ports) on the reduction of the excessive spurious radiation losses is investigated.

II. Method of Analysis

The analysis reported in this paper is based on the two-dimensional planar circuit approach. In this approach, the fringing field at the disk circumference is accounted for by replacing the physical disk by a larger disk surrounded by a perfect magnetic wall. The effective radius a_e of this larger disk is given by [11]

$$a_e = a_0\left\{1+\frac{2d}{\pi\epsilon_r a_0}\left[\ln\left(\frac{\pi a_0}{2d}\right)+1{\cdot}7726\right]\right\}^{1/2} \tag{1}$$

where a_0 represents the physical radius, d is the substrate thickness, and ϵ_r is the dielectric constant of the substrate under the disk. For analysis of similar planar circuits, use of a dynamic permittivity has been suggested by Wolff and Knoppik [5]. Based on this concept, the permittivity used in the analysis of planar resonators is dependent on the field distribution so that different modes possess different dynamic permittivity values. The dielectric constant associated with the lowest order mode of the center-fed disk structure (namely the (0,1) symmetrical mode), however, does not differ significantly from its dynamic permittivity. This can be seen quite clearly from the results report by D'Inzeo *et al.* [6].

A. Z-Matrix of Multiport Disk

The method of analysis is very similar to that of the four-port and five-port microstrip disk circuits discussed previously in [7] and [8]. The two-dimensional impedance Green's function for a circular segment with magnetic walls is available from [9, p. 249]. This Green's function has been used to derive the impedance matrix for the center-fed $(N+1)$-port circular microstrip structure shown in Fig. 1(a). The elements of the Z-matrix are obtained as follows:

$$Z_{ij} = \frac{1}{W_i W_j}\int_{W_i}\int_{W_j} G(s_i/s_j)\, ds_i\, ds_j \tag{2}$$

where W_i and W_j represent the effective widths of ports i and j, respectively, and ds_i, ds_j are incremental distances along the port widths. The effective widths $W_{i,j}$ are related to the effective widths $W'_{i,j}$ of the microstrip lines connected to these ports. The widths $W'_{i,j}$ are related to the impedances $Z_{i,j}$ of the microstrip lines at ports i and j by

$$W'_{i,j} = \frac{\eta d}{\sqrt{\epsilon_{re}}\, Z_{i,j}}. \tag{3}$$

The Green's function G in (2) is given by

$$G(\rho_i,\phi_i;\rho_j,\phi_j) = j\omega\mu d\sum_{n=0}^{\infty}\sum_{m=1}^{\infty} \cdot \frac{\sigma_n J_n(k_{nm}\rho_i)J_n(k_{nm}\rho_j)\cos\left[n(\phi_i-\phi_j)\right]}{\pi\left[a_e^2-\frac{n^2}{k_{nm}^2}\right]\left[k_{nm}^2-k^2\right]J_n^2(k_{nm}a_e)} \tag{4}$$

where k_{nm} are solutions of

$$\left.\frac{\partial}{\partial\rho}J_n(k_{nm}\rho)\right|_{\rho=a_e} = 0. \tag{5}$$

The parameter σ_n equals 1 when $n=0$ and is equal to 2 otherwise. The values of (ρ_i,ϕ_i) and (ρ_j,ϕ_j) specify the locations of the two ports i and j, while the wavenumber k is $\omega\sqrt{\mu_0\epsilon_0\epsilon_r\mu_r}$. The substrate parameters are height d, dielectric constant ϵ_r, and relative permeability μ_r. In order to account for dielectric and conductor losses, the dielectric constant ϵ_r is made complex such that

$$\epsilon_r = \epsilon_{r_0}(1-j\delta_e)$$

where ϵ_{r_0} is the real part of the dielectric constant and δ_e is the effective loss tangent, given by

$$\delta_e = \delta+\delta_c$$

with δ being the loss tangent of the dielectric medium and δ_c representing the additional loss tangent caused by the conductor losses. The factor δ_c is given by $\delta P_c/P_d$, where P_c is the power loss in the conductor and P_d is the power loss in the dielectric. The term δ_c is related to the skin depth of the metallization and is given by

$$\delta_c = \frac{1}{d\sqrt{\mu\pi f\sigma_c}} \tag{6}$$

where σ_c is the conductivity of the metallization.

Upon substituting (4) into (2) and then specifying the port locations, one can determine the impedance matrix elements. For instance, port 1 is located at the center of the disk and its width W_1 is a cylindrical surface of an extent $2\pi\rho_0$, where ρ_0 is the radius of the coaxial feed center conductor. The Z-matrix element Z_{11} corresponding to this port is

$$Z_{11} = \frac{j\omega\mu d}{\pi a_e^2}\sum_{m=1}^{\infty}\frac{J_0^2(k_{0m}\rho_0)}{\left[k_{0m}^2-k^2\right]J_0^2(k_{0m}a_e)}. \tag{7}$$

The other diagonal terms of the impedance matrix (i.e., Z_{ii}

$(i \neq 1))$ are found to be

$$Z_{ii}(i \neq 1) = \frac{2j\omega\mu d a_e^2}{\pi W_i^2} \cdot \sum_{n=0}^{\infty} \sum_{m=1}^{\infty} \frac{\sigma_n \left\{1 - \cos\left[2n \sin^{-1}(W_i'/2a_e)\right]\right\}}{n^2 \left(a_e^2 - \frac{n^2}{k_{nm}^2}\right)\left(k_{nm}^2 - k^2\right)}. \tag{8}$$

Off-diagonal terms in the first row (or the first column) are given by

$$Z_{1j} = \frac{2j\omega\mu d}{\pi a_e W_j} \sum_{m=1}^{\infty} \frac{J_0(k_{0m}\rho_0)\,\Delta_j}{(k_{0m}^2 - k^2) J_0(k_{0m} a_e)} \tag{9a}$$

where Δ_j is the half-angle corresponding to port j (see Fig. 1(b)) and is given by

$$\Delta_j = \sin^{-1}(W_j'/2a_e). \tag{9b}$$

The summation with respect to n does not appear in (7) and (9a) since

$$\int_{\phi_i=0}^{2\pi} \cos\left[n(\phi_i - \phi_j)\right] d\phi_i = \begin{cases} 2\pi & \text{for } n = 0 \\ 0 & \text{otherwise.} \end{cases} \tag{10}$$

The other off-diagonal terms of the Z-matrix are given by

$$Z_{ij}(i \neq 1, j \neq 1) = \frac{2j\omega\mu d a_e^2}{\pi W_i W_j} \cdot \sum_{n=0}^{\infty} \sum_{m=1}^{\infty} \frac{\sigma_n}{n^2 \left[a_e^2 - \frac{n^2}{k_{nm}^2}\right]\left[k_{nm}^2 - k^2\right]} \cdot \left\{\cos\left[n(\Delta_i - \Delta_j)\right] - \cos\left[n(\Delta_i + \Delta_j)\right]\right\} \cdot \cos(n\phi_{ij}). \tag{11}$$

The two expressions given in (8) and (11) are identical to the corresponding expressions derived in [7] and [8]. The impedance matrix obtained from (7) through (11) is then converted into the more familiar S-matrix representation.

B. Additional Shorted Ports along the Circumference

Preliminary measurements on power divider circuits with a small number of circumferential output ports (typically three) have shown the existence of excessive spurious losses. These losses decrease considerably when additional shorted ports are introduced between the adjacent output ports along the disk circumference as shown in Fig. 2. Due to the practical limitations imposed by the fabrication process, those shorted ports are generally inductive and hence possess nonzero impedance values. A general approach for this problem would be to consider a microstrip disk with "$m-1$" circumferential ports. An "s" number of these ports will be treated as being terminated by loads of arbitrary impedance values. Following the method of analysis outlined above in subsection A, an m by m impedance matrix characterizing this circuit can be obtained. This m by m Z-matrix may be partitioned as

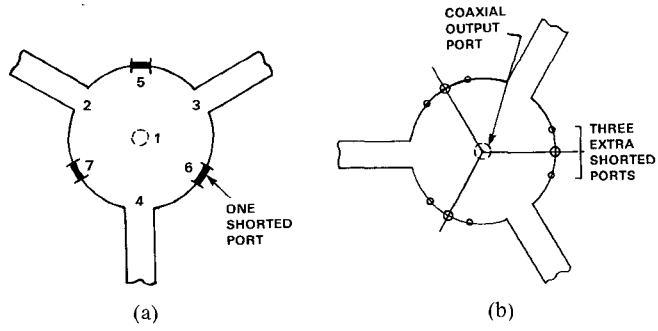

Fig. 2. (a) A center-fed microstrip disk three-way power divider with three extra shorted ports around the circumference. (b) A three-way power combiner circuit using nine extra shorted ports.

$$\tilde{Z}_{(m\times m)} = \begin{bmatrix} \tilde{Z}_{pp} & \tilde{Z}_{pl} \\ \tilde{Z}_{lp} & \tilde{Z}_{ll} \end{bmatrix} \tag{12}$$

where the dimensions of the submatrices $\tilde{Z}_{pp}$, $\tilde{Z}_{pl}$, $\tilde{Z}_{lp}$, and $\tilde{Z}_{ll}$ are $\{(m-s),(m-s)\}$, $\{(m-s), s\}$, $\{s,(m-s)\}$, and $\{s, s\}$, respectively. Voltages and currents at various ports are related by

$$\bar{V}_p = \tilde{Z}_{pp}\bar{I}_p + \tilde{Z}_{pl}\bar{I}_l \tag{13}$$

and

$$\bar{V}_l = \tilde{Z}_{lp}\bar{I}_p + \tilde{Z}_{ll}\bar{I}_l \tag{14}$$

where $\bar{V}_p$ is a vector representing voltages at $(m-s)$ external ports, $\bar{I}_p$ represents currents flowing into these external ports, and $\bar{V}_l, \bar{I}_l$ are, respectively, voltages and currents for the "s" terminated ports. If the impedances terminating these "s" ports are presented by a diagonal matrix $\tilde{Z}_{LL}$, then

$$\bar{V}_l = -\tilde{Z}_{LL}\bar{I}_l. \tag{15}$$

By substituting (15) into (14), we obtain an expression for $\bar{I}_l$ in terms of $\bar{I}_p$. This expression, together with (13), yields

$$\bar{V}_p = \left\{\tilde{Z}_{pp} - \tilde{Z}_{pl}\left[\tilde{Z}_{LL} + \tilde{Z}_{ll}\right]^{-1}\tilde{Z}_{lp}\right\}\bar{I}_p. \tag{16}$$

Thus the $(m-s)$ by $(m-s)$ Z-matrix for the external ports may be written as

$$\tilde{Z} = \tilde{Z}_{pp} - \tilde{Z}_{pl}\left(\tilde{Z}_{LL} + \tilde{Z}_{ll}\right)^{-1}\tilde{Z}_{lp}. \tag{17}$$

In the ideal case where the terminating loads have zero impedance, (17) reduces to

$$\tilde{Z} = \tilde{Z}_{pp} - \tilde{Z}_{pl}\tilde{Z}_{ll}^{-1}\tilde{Z}_{lp}. \tag{18}$$

For the special case of a three-way power divider, shown in Fig. 2(a), $m = 7$ and $s = 3$, and $\tilde{Z}$ in (17) and (18) is a 4×4 impedance matrix.

III. Numerical and Experimental Results

The method of analysis described in the previous section has been used to analyze the various multiport power divider geometries shown in Fig. 3. In this section we present the measured performance and the calculated results of these geometries.

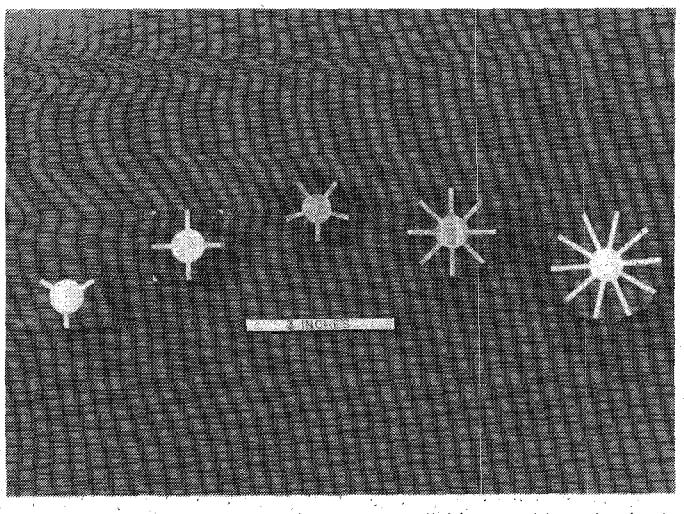

Fig. 3. Photo of various multiport power divider/combiner circuits.

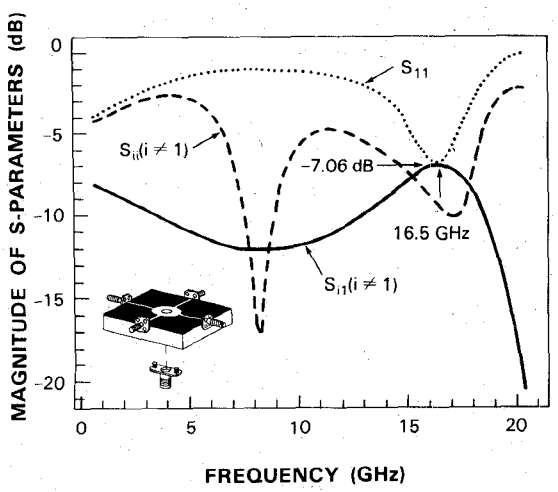

Fig. 4. Theoretical results for a center-fed four-way power divider (disk radius = 7.5 mm).

Throughout this section we have assumed that the circumferential ports are symmetrically located around the disk. Additionally, the frequency variation of Z_0 and W_e (the effective width of the microstrip lines) has been taken into account. Furthermore, the dielectric losses are included in the theoretical computations while the conductor losses are neglected. Finally, in the numerical computation of Z_{ij} it has been found that convergence occurs by selecting n and m to be equal to 20 each.

A. A Four-Way Power Divider Circuit

A center-fed four-way power-divider is shown in the Fig. 4 insert. The S-parameters of this configuration have been calculated over the frequency range 1 GHz to 20 GHz and are plotted in Fig. 4. These results have been computed for a circular disk with a 7.50 mm radius. The radius of the circular disk depends upon the frequency of operation and is determined by (5). The substrate is 31 mil thick and has a dielectric constant $\epsilon_r = 2.2$. The characteristic impedance of the output ports are taken to be 50 Ω.

TABLE I
EFFECT OF THE CHARACTERISTIC IMPEDANCE OF THE OUTPUT LINES ON THE CHARACTERISTICS OF A FOUR-WAY CENTER-FED POWER DIVIDER CIRCUIT WITH A DISK RADIUS OF 8.65 MM

Z_0	S_{j1}	S_{11}	FREQUENCY	BANDWIDTH $\lvert S_{21}\rvert < 7$ dB, $\lvert S_{11}\rvert > 7$ dB
60	-6.99	-7.26	14.5 GHz	300 MHz
55	-6.89	-7.70	14.5 GHz	700 MHz
50	-6.79	-8.21	14.5 GHz	800 MHz
45	-6.68	-8.85	14.5 GHz	1000 MHz
40	-6.54	-9.67	14.7 GHz	1400 MHz
35	-6.39	-11.15	14.7 GHz	1900 MHz
30	-6.20	-15.00	14.9 GHz	2100 MHz

Inspection of the computed results reveals that the return loss S_{11} of the feed port is minimum at 16.5 GHz. This frequency is near 15.43 GHz, which is the resonance frequency of the (0,1) mode of the circular disk cavity structure. The transmission coefficient from the center port to any of the circumferential ports (at 15.43 GHz) is −7.06 dB. For an ideal power divider this value should be −6.0 dB. The dependence of the transmission coefficient on the characteristic impedance of the output ports has been studied and the results are presented in Table I. These results clearly indicate that both the reflection and the transmission coefficients improve monotonically when the characteristic impedance Z_0 for the output ports is varied from 60 Ω to 30 Ω. Bandwidth values for various Z_0's are also shown in this table. As there is no standard definition for the bandwidth of power dividers, the values shown here are computed for $|S_{21}| < 7$ dB (1 dB more than the nominal value of 6 dB) and $|S_{11}| > 7$ dB (i.e., VSWR < 2.6). These numbers are good only for relative comparison. One should note here, however, that when the port widths are increased (i.e., Z_0 decreased), a considerable improvement in bandwidth can be obtained. Furthermore it should be emphasized that the effect of the impedance-matching sections on bandwidths is not included in these computations.

Experimental results for a four-way power divider fabricated on 31 mil Duroid ($\epsilon_r = 2.2$) substrate with disk radius of 7.5 mm are shown in Fig. 5. For sake of comparison, the theoretical calculations are also shown. In general the agreement is fairly good. However, we note that the measured value of S_{11} at 16.34 GHz is much better than the corresponding theoretical value. This feature has been also observed for other geometries, but the discrepancy becomes smaller as one increases the number of ports along the circumference. This point is discussed further in subsection B, where the performance for circuits with different number of ports is compared.

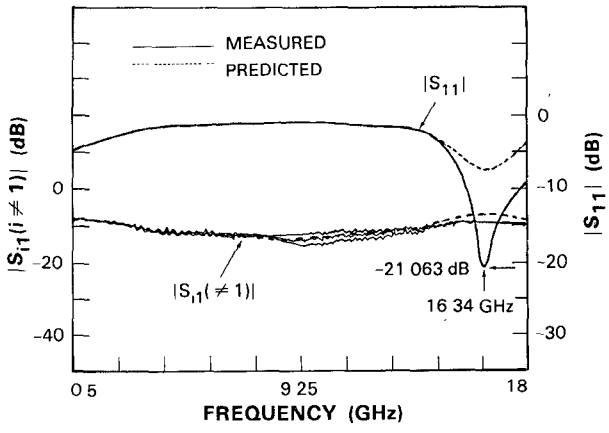

Fig. 5. Typical results for a four-way center-fed microstrip disk power divider (disk radius = 7.5 mm).

TABLE II
COMPARISON OF S_{11} AT CENTER-FED COAXIAL PORT FOR DIFFERENT VALUES OF N AND FOR A DISK RADIUS OF 8.65 MM

NUMBER OF PORTS ON CIRCUMFERENCE	$\|S_{11}\|$ EXPERIMENTAL dB	$\|S_{11}\|$ THEORETICAL dB
4	-21.07	- 8.2
5	-18.72	-19.0
8	- 9.85	-12.37
10	- 9.82	- 9.50

TABLE III
TRANSMISSION COEFFICIENT VALUES FOR THREE, FOUR, FIVE, EIGHT, AND TEN WAY POWER DIVIDERS WITH 8.65 MM DISK RADIUS

N-WAY DIVIDER	S_{21} (Expt)	S_{21} (Ideal)	EXTRA LOSS*	CALCULATED S_{21}
N = 3	-10 dB	-4.77 dB	5.23 dB	—
N = 4	-9 dB	-6.0 dB	3.0 dB	-6.8 dB
N = 5	-9.0 dB	-7.0 dB	2.0 dB	-7.08 dB
N = 8	-10 dB	-9 dB	1.0 dB	-9.31 dB
N = 10	-11 dB	-10 dB	1.0 dB	-10.54 dB

*Extra loss = S_{21}(ideal) − S_{21}(expt.).

B. Comparison of Circuits with Different Values of N

Numerical computations have been carried out and experiments have been performed on a number of circuits with three, four, five, eight, and ten ports along the circumference. Calculated and measured values of S_{11} are compared in Table II, whereas values of S_{21} are compared in Table III.

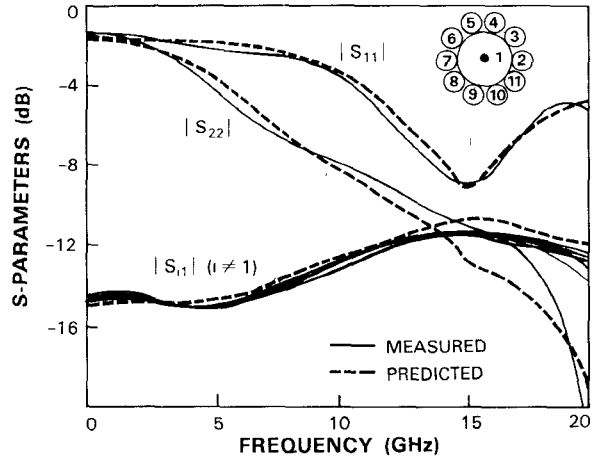

Fig. 6. Predicted and measured performance of a ten-way power divider/combiner center-fed microstrip disk circuit with disk radius = 8.65 mm.

As we have mentioned earlier, the experimental values of S_{11} are, in general, better than the theoretically calculated values (except for $N = 8$). It is believed that this behavior is caused by the radiation loss associated with the fringing fields at the circular edge of the disk. This radiation loss (which is not accounted for in the analysis) causes a reduction in the reflection coefficient at the resonance frequency. As the number of circumferential ports is increased, the exposed edge of the disk and hence the radiated power become smaller. Thus, better agreement between theory and experiment for disks with larger number of ports (about eight ports or more) would be expected.

In addition to the calculated and measured values of S_{21}, Table III includes the ideal values (for perfect divider/combiner circuits) also. An extra loss defined as the difference between the experimental and ideal S_{21} values is also included. This extra loss decreases as the number of ports along the circumference is increased. This again can be explained in terms of radiation from the open edges along the disk circumference. Since our calculations do not take this radiation into account, the calculated values are close to the ideal values.

In view of the above observations, one may conclude that the design approach presented in this paper is more suitable for disks with larger number of ports (eight or more) along the circumference.

C. Ten-Way Power Divider/Combiner Circuit

The calculated and measured behavior of a ten-way power divider circuit is shown in Fig. 6. The calculated results are obtained by following the computational procedure outlined in Section II of this paper. The effective disk radius, however, is taken to be equal to the physical radius. This is because most of the disk circumference is covered by the outgoing microstrip lines and hence field fringing effects will be negligible. In order to characterize the performance of this circuit a successive set of scattering parameters measurements were taken. The effects of the SMA connectors were gated out by using the

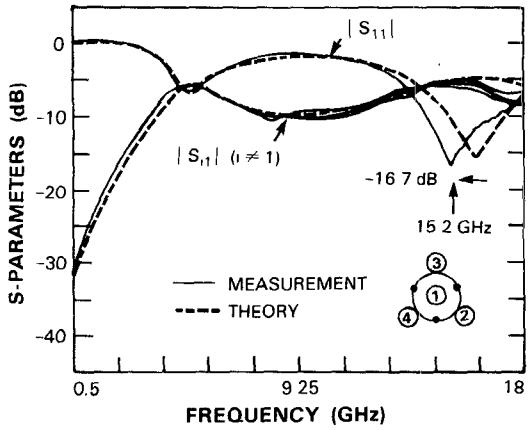

Fig. 7. Predicted and measured characteristics of a three-way divider/combiner circuit with three shorted ports (disk radius = 8.65 mm.)

time-domain feature on the automatic network analyzer. In addition to the close agreement between the measured and the computed data of this circuit, it has been noted that this circuit is also suitable as a power combiner. The measured return loss at any circumferential port, and the isolation between any two circumferential ports (adjacent, straight across, or otherwise) were found to be, respectively, no less than −14 dB (VSWR = 1.5) and −11 dB at 17 GHz. Over a frequency range of 15 to 20 GHz, the corresponding values are better than −12.6 dB and −9 dB, respectively. This performance was achieved without using any computer or experimental optimization. A better performance may be achieved if a design optimization is carried out.

Finally, it should be noted that in the power combiner design presented above, no external isolation resistances were used. Indeed, it is this property that makes this design geometry substantially more attractive than other radial combiners [2].

D. Three-Way Power Divider Circuit with Additional Shorted Ports

As mentioned earlier, Table III lists the ideal, calculated, and measured transmission characteristics of a number of power divider circuits. The extra loss reported in this table is defined as being the difference between the ideal and the measured transmission coefficients S_{21}. This loss is unacceptably large for small values of N and it is believed to be caused, at least in part, by the radiation losses at the exposed edges along the disk circumference.

Incorporation of additional short-circuited ports along the disk circumference (and half way between every two adjacent output ports) has caused a significant reduction in these extra losses. Two examples of this modified three-way power divider configuration is shown in Fig. 2. The measured characteristics of the modified circuit depicted in Fig. 2(a) is shown in Fig. 7. By incorporating three additional ports, we were able to reduce the extra loss from 5.23 dB to only 0.24 dB and hence an acceptable performance has been achieved. The theoretical characteristics of this divider were calculated via the formulations of Section II-B and are included in Fig. 7. Very good agreement between the predicted and the measured results is obtained.

Based on these results it appears that the inclusion of shorted ports along the disk circumference would be a useful technique for improving the performance of multiport circuits, especially those with small number of circumferential ports.

IV. Concluding Remarks

A general method for the analysis and design of a multiway circular microstrip disk power divider/combiner circuits has been described. This method is based on the planar circuit approach. In this approach the two-dimensional Green's function for the circular segment is used to derive the impedance matrix of the circuit. Theoretical and experimental results for three-way, four-way, five-way, eight-way, and ten-way power divider/combiner circuits have been reported. The measured results are in good agreement with the calculated results. Two attractive features for this design approach have been discovered. First, a ten-way power divider/combiner circuit can be realized without the need for discrete isolation resistances, and secondly, the incorporation of the extra shorted ports around the disk circumference of a three-way power divider has been shown to be very effective in reducing the spurious radiation losses.

In the circuit configurations discussed in this paper, the widths of the circumferential ports are determined by the characteristic impedances of the feed lines (usually 50 Ω). An increased flexibility can, however, be obtained if these widths were treated as design parameters and adjusted to obtain optimum performance. As discussed in Section III-A, increasing the widths of the circumferential ports of a four-way power divider could reduce the excessive spurious losses and improve the input match at the center-feed coaxial port. However, when the widths of the circumferential ports are different from those of the microstrip feed lines, impedance-matching sections will be needed. The segmentation method [9] can then be used for analysing this modified configuration. As discussed in [8], the matching sections are treated as rectangular planar segments connected to the circular disk. The impedance matrix Z_r for each of the rectangular segments is obtained via the procedure outlined in [10], while the impedance matrix Z_c of the circular disk segment is computed following the procedure described in Section II-A.

Finally, it should be noted (for the various geometries reported in this paper) that no efforts were made to optimize the performance of the circuits, and hence all of the results cited should be considered only as samples of the potential performance that could be achieved from these types of circuits. A systematic design optimization should yield much superior performance.

Acknowledgment

Many thanks are due to K. A. Telley for typing the manuscript and to J. Austin for performing the measurements.

REFERENCES

[1] Adel A. M. Saleh, "Planar electrically symmetric *N*-way Hybrid Power Dividers/Combiners," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 555–563, June 1980.

[2] S. J. Foti, R. P. Flam, and W. J. Scharpf, "60-way radial combiner uses no isolator," *Microwaves and RF*, pp. 96–118, July 1984.

[3] E. Belohoubek *et al.*, "30-way power combiner for miniature GaAs FET power amplifiers," in *1986 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 515–518.

[4] A. Fathy and D. Kalokitis, "Analysis and design of a 30-way radial combiner for the *Ku*-band applications," *RCA Rev.*, vol. 47, pp. 487–508, Dec. 1986.

[5] I. Wolff and N. Knoppik, "Rectangular microstrip disc capacitors and resonators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 857–864, Oct. 1974.

[6] G. D'Inzeo, F. Giannini, C. M. Sodi, and R. Sorrentino, "Method of analysis and filtering properties of microwave planar networks," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 462–471, July 1978.

[7] M. D. Abouzahra and K. C. Gupta, "Analysis and design of five-port circular disc structure for six-port analyzers," in *1985 IEEE MTT Int. Microwave Symp. Dig.*, pp. 449–452.

[8] K. C. Gupta and M. D. Abouzahra, "Analysis and design of four-port and five-port microstrip disc circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1422–1427, Dec. 1985.

[9] K. C. Gupta *et al.*, *Computer-Aided Design of Microwave Circuits*. Dedham MA: Artech House, 1981, p. 249.

[10] A. Benalla and K. C. Gupta, "Faster computation of *Z*-matrices for rectangular segments in planar microstrip circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 733–736, June 1986.

[11] W. C. Chew and J. A. Kong, "Effects of fringing fields on the capacitance of circular microstrip disk," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 98–103, Feb. 1980.

✠

Mohamed D. Abouzahra (S'79–M'85–SM'87) was born in Beirut, Lebanon, on June 15, 1953. He received the B.S. degree (with distinction) in electronics and communications from Cairo University, Cairo, Egypt, in 1976 and the M.S. and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, in 1978 and 1984, respectively.

From 1979 to 1984 he worked as a research and teaching assistant at the University of Colorado, Boulder. Since 1984 he has been a member of the Countermeasures Technology group at the Massachusetts Institute of Technology, Lincoln Laboratory. He has worked on microstrip line discontinuities, wide-band dielectric directional couplers, and dielectric image lines. He is currently interested in the computer-aided design of microwave and millimeter-wave wide-band planar circuits, and in the development of wide-band automated measurement schemes for characterizing composite materials.

✠

Kuldip C. Gupta (M'62–SM'74) received the B.S. and M.S. degrees in electrical communication engineering from the Indian Institute of Science, Bangalore, India, in 1961 and 1962, respectively, and the Ph.D. degree from the Birla Institute of Technology and Science, Pilani, India, in 1969.

Dr. Gupta has been at the University of Colorado since 1983, initially as a Visiting Professor and later as a full Professor. Earlier he had a long stay (since 1969) at the Indian Institute of Technology, Kanpur (India), where he had been a full Professor of Electrical Engineering since 1975. On leave from IITK, he has been a Visiting Professor at the University of Waterloo, Canada; at the Ecole Polytechnique Federale de Lausanne, Switzerland; at the Technical University of Denmark (Lyngby); at the Eidgenossische Technische Hochschule, Zurich; and at the University of Kansas, Lawrence. From 1971 to 1979 he was the Coordinator for the Phased Array Radar Group of the Advanced Center for Electronics Systems at the Indian Institute of Technology.

Dr. Gupta's current research interests are in the area of computer-aided design techniques for microwave/millimeter-wave integrated circuits and integrated antennas. He is author/coauthor of four books: *Microwave Integrated Circuits* (Wiley Eastern, 1974; Halsted Press of John Wiley, 1974), *Microstrip Lines and Slotlines* (Artech House, 1979), *Microwave* (Wiley Eastern, 1979; Halsted Press of John Wiley, 1980; Editorial Limusa Mexico, 1983), and *CAD of Microwave Circuits* (Artech House, 1981; Chinese Scientific Press, 1986). Also, Dr. Gupta has contributed chapters to the forthcoming *Handbook of Microstrip Antennas* (Peter Peregrinus) and *Handbook of Microwave and Optical Components* (John Wiley). He has published over 100 research papers and holds one patent in the microwave area. Dr. Gupta is a Fellow of the Institution of Electronics and Telecommunication Engineers (India). He is on MTT-S Technical Committee on CAD, on the Editorial Board for MTT-S Transactions, and on the Technical Program Committee for MTT-S International Symposia. He is a Guest Editor for a forthcoming Special Issue of MTT Transactions on Computer-Aided Design.